REMARKS/ARGUMENTS

Claims 1 – 8, 10, and 13 have been canceled and the limitations of claims 10 and 13 have been incorporated into claim 9.

The rejection of claims 9 and 11 – 14 under 35 U.S.C. § 103(a) as being unpatentable over Juskey et al. in view of Edwards et al., and to the extent applicable to claim 9, the rejection under 35 U.S.C. § 103(a) as being unpatentable over Juskey et al. in view of Edwards et al. and further in view of Dolbear, are both respectfully traversed.

A comparison of the present invention and the citations reveals the following significant technical differences.

In the heat sink structure of the present invention, a plurality of recessed cavities are formed on a lower surface of a heat sink, wherein at least one electronic component is embedded in at least one of the recessed cavities, allowing at least one of the other recessed cavities to receive at least one active component such as semiconductor chip; the heat sink structure can be mounted on a substrate. Although Juskey et al. teach a package 5 with a single semiconductor chip 16 and a heat sink 20, and Dolbear teaches a package with a single semiconductor chip 42 and a heat sink 46 having a hole 72 for receiving a chip, however neither Juskey et al. nor Dolbear discloses a heat sink embedded with electronic components such as passive components to improve the overall electrical performance of the semiconductor package.

Although Edwards et al. teach a semiconductor package with a plurality of chips and a heat sink 50 mounted on a substrate 10 and the chips, however they do not disclose embedding electronic components in recessed cavities on a lower surface of the heat sink. In the present invention, the electronic components are embedded in the recessed cavities of the heat sink, and the heat sink is further formed with at least one through hole, such that when the heat sink is mounted on the substrate, the semiconductor chip can be received in the through hole. By such arrangement, the heat sink with the electronic components being embedded in the recessed cavities thereof and the substrate with the semiconductor chip being mounted on the surface thereof are combined together to form the semiconductor package, such that the heat sink and the substrate can be fabricated separately to

simplify the fabrication processes, and the quality of the heat sink and the substrate can be assured before being combined together. However for Edwards et al., as long as any one component is defective, the entire structure does not function properly.

Moreover, the heat sink of the present invention is embedded with the electronic components, and the electronic components are mounted on the substrate, such that the heat sink is connected to the substrate by the electronic components. However, the cited references each use an encapsulating compound to connect the heat sink to the substrate. Thus, the cited references each employ a different method for connecting the heat sink to the substrate as compared to that of the present invention, such that cited references cannot render the present invention obvious.

Therefore, the cited references alone cannot anticipate a structure of a heat sink with electronic components being embedded in recessed cavities on a lower surface thereof, and a combination of the cited references does not directly teach or suggest the structural features of the present invention. It is believed that the present invention is patentable over the citations according to the above comments and should be allowed.

Accordingly a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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